LDA TECHNOLOGIES™

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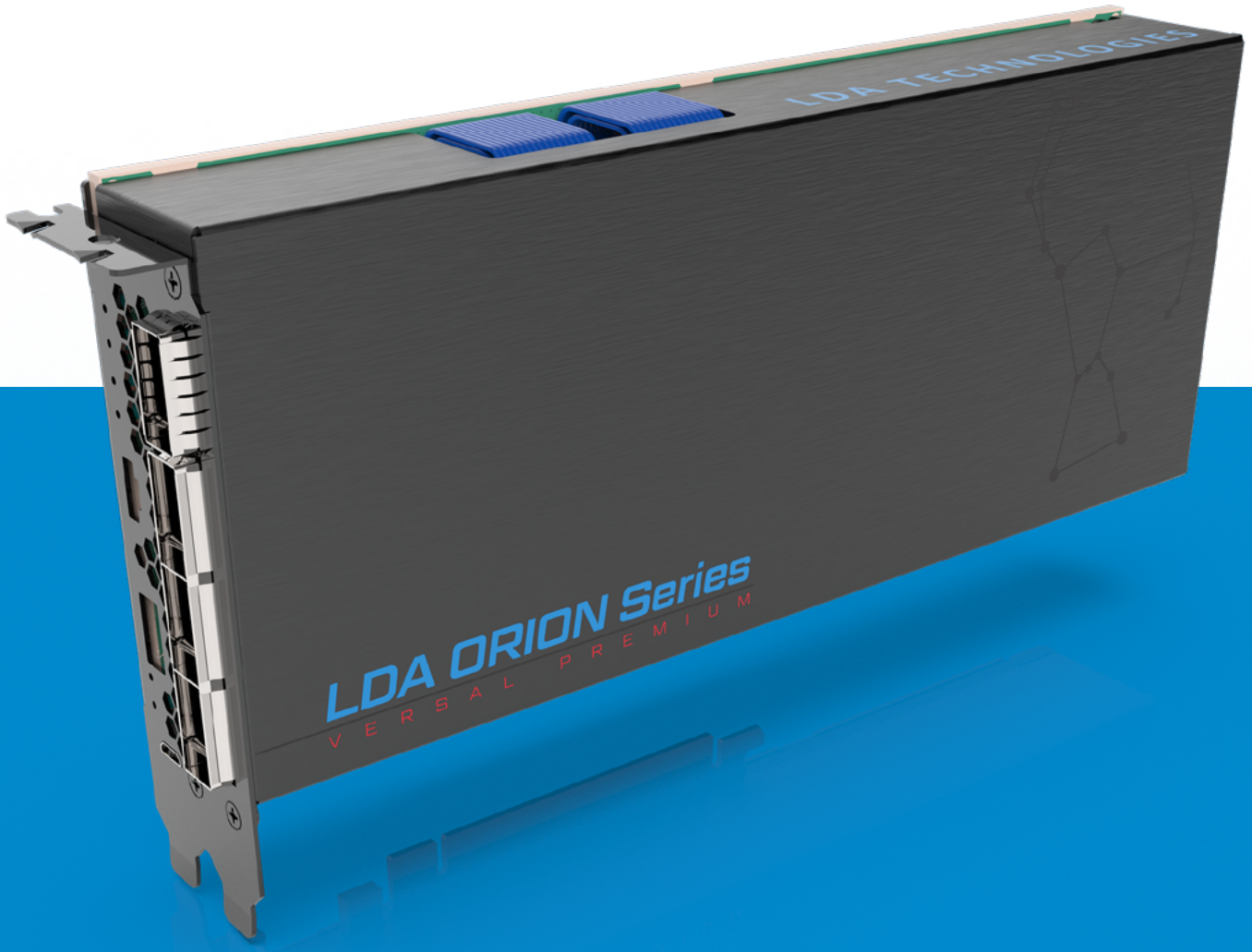


LDA ORION Series

DATASHEET

LDA Orion Series

PCIe Standard ¾ length board with Xilinx Versal Premium **XCVP1202VSVA2795-3-ES1** or **XCVP1502VSVA2795-3-ES1** Engineering Silicon FPGA.

The Versal VP1202/VP1502 chip is the next generation Xilinx FPGA designed for ultra-high-performance applications such as machine learning, complex simulations, high-frequency trading, programmable networking, cryptography, and data center applications.

VP1202 chip highlights:

- System Logic Cells: 1,969 million
- Total Block RAM: 47 Mb
- UltraRAM: 190 Mb
- DSP Engines: 3,984
- 100G Multirate Ethernet MAC: 2

VP1502 chip highlights:

- System Logic Cells: 3.763 million
- Total Block RAM: 89 Mb
- UltraRAM: 366 Mb
- DSP Engines: 7,440
- 100G Multirate Ethernet MAC: 4

The board is featuring 432 MB of ultra-low-latency GSI SRAMs delivering over 290 Gbps of memory bandwidth with ultra-low random-access latency.

8 GB of LPDDR4 memory running at 4266 MHz is provided as a general bulk memory for ARM processing subsystem.

The board is offered with multiple I/O cards supporting a variety of I/O interfaces such as QSFP, QSFP-DD, SFP28 ports. The I/O interface pinout and all mechanical/electrical specifications are available to customers for designing their own custom I/O cards.

PCIE

The PCIe interface supports the following modes of operation:

- PCIe 3.0 x16 or bifurcated 2x8
- PCIe 4.0 x16 or bifurcated 2x8
- Bifurcated 2x PCIe 5.0 x8
- Multi-hosting (contact LDA for more information)

SRAM

Twelve GS82583ET18GK-675 SRAM chips installed on the board provide 18-bit / 288 Mbit / 675 MHz memory with read latency of 3 clocks. Six independent memory channels, each memory controller bonds two SRAM chips together providing a 576 Mb with 36-bit interface.

The user application side is running at up to 515 MHz (higher clock rates are pending characterization) providing 23-bit address bus and 72-bit data bus per memory controller. Each memory controller supports ~38 Gbps bandwidth (at 515Mhz clock).

- Total SRAM capacity is 3.456 Gb (432 MB).
- Total SRAM bandwidth 222 Gbps (27.8 GBps).
- Six clock cycles read latency. 11.6 ns at 515 Mhz.
- Three clock cycles read/write and write/read bus turnaround latency.
- Completely random read write access.
- No Read/Write bursts requirement to achieve maximum performance.
- Software driven calibration implemented in BMC (very low fpga CLB utilization).
- Per controller sleep mode.

I/O CARD

The launch I/O card for the board supports following interfaces:

- 3x QSFP-DD
- 1x QSFP

Total of 28 interfaces. 20 GTM transceivers supporting rates up to 56 Gbps PAM4 or 28 Gbps NRZ. 8 GTYP transceivers supporting up to 28 Gbps NRZ data rate.

I/O CARDS IN DEVELOPMENT

- 6x SFP: Straight six SFP+ ports connected to GTYP transceivers.
- 4x QSFP: 2x QSFP connected to GTM, 2x QSFP connected to GTYP.
- L1-10G: 1x QSFP, 2x QSFP-DD.
  1 ns latency full-mesh 10 Gbps L1 fabric.
- L1-25G: 2x QSFP. <2 ns latency full mesh 25 Gbps L1 fabric.

ARC6

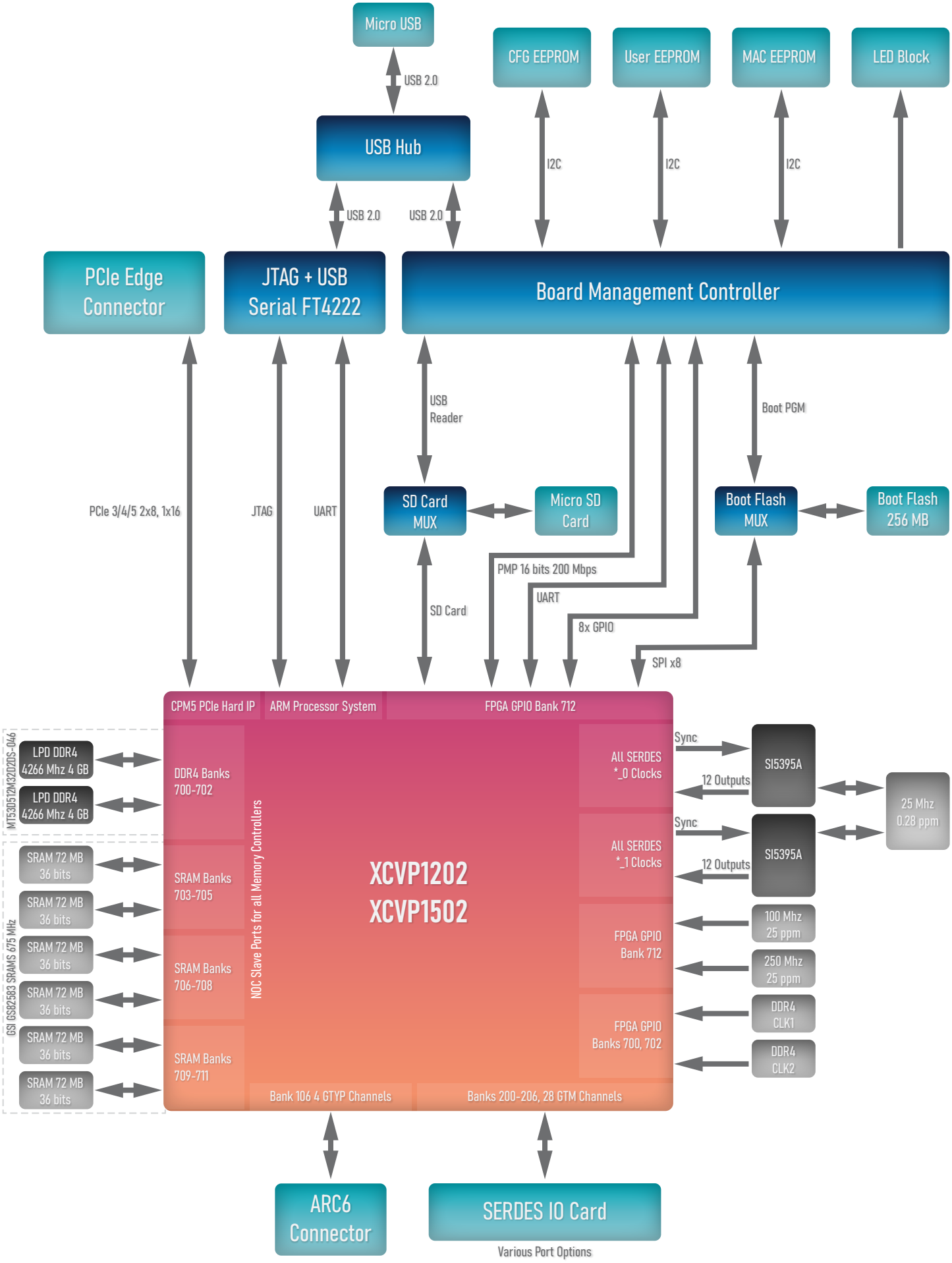
Samtec AcceleRate® Connector provides a dedicated backplane port for local NIC connectivity. Such connection enables LDA TCP offload and NetRecap IP cores operation. ARC6 connector is connected to GTYP BANK 106. LDA provides a variety of pigtail adapters converting ARC6 to QSFP transceiver, ARC6 to SFP copper transceivers, or ARC6 to QSFP cage that can host a regular 10, 40 and 100 Gbps fiber optics. This port exposes 4 SerDes channels in addition to the I/O card.

DDR4

Two Micron LPDDR4 4 GB on-board memory chips are connected to NOC supporting hard IP memory controller. The ARM processing subsystem can use it as a native RAM.

The total DDR4 capacity is 8 GB.

The total DDR4 interface width is 64 bits.


Micro USB
USB 2.0
USB Hub
USB 2.0
USB 2.0
CFG EEPROM
User EEPROM
MAC EEPROM
LED Block
I2C
I2C
I2C
PCIe Edge Connector
JTAG + USB Serial FT4222
Board Management Controller
PCIe 3/4/5 2x8, 1x16
JTAG
UART
USB Reader
SD Card MUX
Micro SD Card
SD Card
Boot PGM
Boot Flash MUX
Boot Flash 256 MB
PMP 16 bits 200 Mbps
UART
8x GPIO
SPI x8
CPM5 PCIe Hard IP
ARM Processor System
FPGA GPIO Bank 712
MT53D512M32D2DS-046
LPD DDR4 4266 Mhz 4 GB
LPD DDR4 4266 Mhz 4 GB
DDR4 Banks 700-702
GSI GS82583 SRAMS 675 MHz
SRAM 72 MB 36 bits
SRAM 72 MB 36 bits
SRAM 72 MB 36 bits
SRAM 72 MB 36 bits
SRAM 72 MB 36 bits
SRAM 72 MB 36 bits
SRAM Banks 703-705
SRAM Banks 706-708
SRAM Banks 709-711
NOC Slave Ports for all Memory Controllers
XCVP1202
XCVP1502
All SERDES *_0 Clocks
All SERDES *_1 Clocks
FPGA GPIO Bank 712
FPGA GPIO Banks 700, 702
Bank 106 4 GTYP Channels
Banks 200-206, 28 GTM Channels
Sync
12 Outputs
SI5395A
Sync
12 Outputs
SI5395A
25 Mhz 0.28 ppm
100 Mhz 25 ppm
250 Mhz 25 ppm
DDR4 CLK1
DDR4 CLK2
ARC6 Connector
SERDES IO Card
Various Port Options

BMC

Powerful Board Management Controller (BMC) with onboard CLI and Python API provides flexible and straightforward board management and monitoring.

- Onboard CLI.
- Python, C++ API.
- 200 Mbps parallel port connected to the FPGA fabric and the NOC.
- USB SD Card Reader for simple OS images transfer to ARM processors.
- Fast FPGA Boot Flash programming.
- Temperature, voltage, current monitoring.
- SNMP agent for centralized management.
- Dedicated preprogrammed array of 32 MAC addresses.
- I/O ports monitoring. Full QSFP, SFP, QSFP-DD access and programming through CLI and API.
- CLI-based clock selection supporting custom clock configurations.

CLOCKING

- Two Identical Si5395A programmable ultra-low-jitter reference clock generators and jitter attenuators providing reference clock source to every FPGA Serdes bank and SRAM memory controllers.
- Standalone 100 MHz 25 ppm programmable SI570 clock generators for each LPDDR4 controller.
- PCIe 5.0 compatible PI6CB33401ZHIEX jitter attenuator supporting bifurcation and multi-hosting scenarios.
- Fixed 100 MHz 25 ppm clock source for PCIe Hard IP.
- Fixed 100 MHz 25 ppm utility clock source for FPGA logic.
- Fixed 250 MHz 25 ppm utility clock source for FPGA logic.

MECHANICAL

Board can operate with or without I/O card. When I/O card is not installed, only ARC6 interface is available (4 SerDes channels total).

OPTIONS WITHOUT I/O CARD

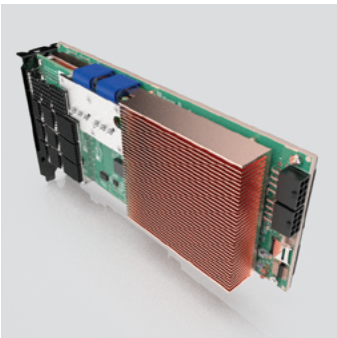
- ¾ length, full height, single slot. Up to 150 Watts power consumption with forced air setup in typical 2U Server.
- ¾ length, full height, double slot. Up to 350 Watts power consumption with forced air setup in typical 2U Server.

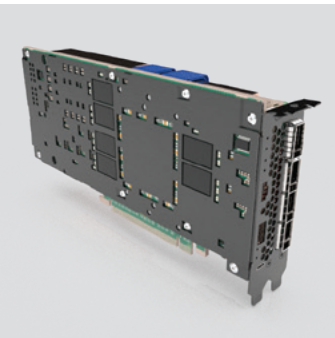
OPTIONS WITH I/O CARD

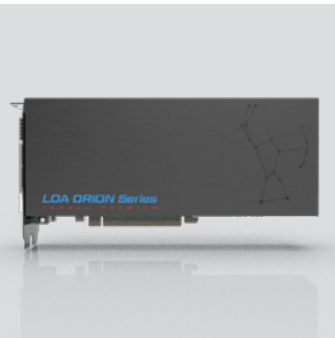
- ¾ length, full height, double slot. Up to 250 Watts power consumption with forced air setup in typical 2U Server.

UNCONVENTIONAL I/O CARD LOCATION

The I/O card design allows for its relocation to other PCIe slots of a server i.e., it does not necessarily need to be part of FPGA board assembly. For example, it can utilize adjacent slot in the server when double-slot PCIe sockets are not available. Contact LDA for more information.







POWER

All PMIC voltage regulators are built using Monolithic Power Systems MPM36xx chipset. Each voltage regulator is monitored in real time for overload and overtemperature errors.

VCORE power rail voltage can be adjusted runtime (reduced from nominal) using CLI or Python API for power saving.

The accurate power monitor is implemented for PCIe edge connector as well as each 8 Pin auxiliary power connectors.