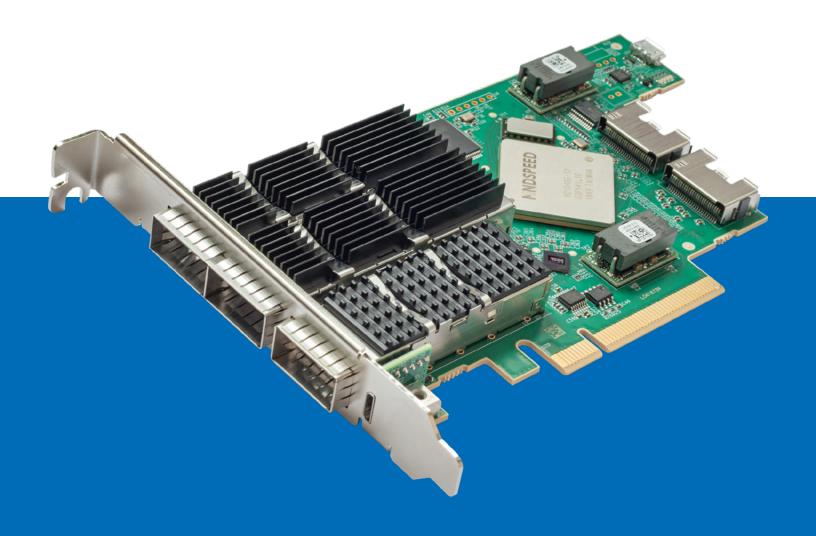


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# LDA D6 Mark II DATASHEET

# LDA D6 Mark II Layer 1 Server Add-on

D6 Mark II is a PCIe card that provides Layer 1 switching with sub-nanosecond roundtrip latency. The card has two QSFPDD and one QSFP ports at the front and two AcceleRate® Slim Sockets at the back: 36 10 G lanes in total with full mesh interconnect. AcceleRate sockets allow connecting D6 to an FPGA board installed in the same server or interconnecting multiple D6 cards to form a daisy chain of Layer 1 fabrics.

### HIGHLIGHTS

- Roundtrip Latency: down to 0.73 nanoseconds
- Layer 1: Full mesh for 36 12.5 Gbps lanes
- Ports: 2x QSFP DD and 1x QSFP
- AUX connectors: 2x AcceleRate® Slim Socket

#### MANAGEMENT

- Management controller with onboard CLI and API.
- Management ports\*:
  - Micro USB in the front
  - Micro USB in the back
  - PCIE SMBUS
  - \*All management ports are accessible in parallel.
- Onboard QSFP, QSFPDD Diagnostics software

#### MECHANICAL

- 152 mm / 6" length
- 86 mm / 3.38" height
- Single slot

## **QSFP ULL MODES**

- Dedicated CDR circuitry on QSFP port.
- When CDR is disabled, QSFP operates in ultra-low-latency mode.
- Enabling CDR increases Layer 1 latency by 0.45 ns in each direction.
- One-way\* latencies\*\* of QSFP lanes (ns) per ULL mode:

	ULL FULL / CDR OFF	ULL RX / CDR TX ON	ULL TX / CDR RX ON	ULL OFF / CDR ON
QSFP Lane 1	0.5330	0.7755	0.7755	1.0020
QSFP Lane 2	0.5495	0.7915	0.7915	1.0180
QSFP Lane 3	0.5980	0.8240	0.8240	1.0505
QSFP Lane 4	0.5980	0.8405	0.8405	1.0665

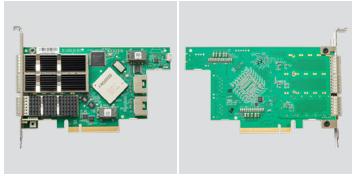
#### PORT LATENCY ANALYSIS

Per-port per-lane per-direction latencies\* are given in the table below. To get a roundtrip latency on any given route, corresponding RX and TX latency numbers have to be summed up.

Port	Lane	RX Latency (ns)	TX Latency (ns)
	Lane 1	0.5315	0.5345
QSFP	Lane 2	0.5480	0.5510
QSFP	Lane 3	0.5965	0.5995
	Lane 4	0.5965	0.5995
	Lane 5	0.3705	0.3735
	Lane 6	0.3545	0.3575
	Lane 7	0.3545	0.3575
	Lane 8	0.3540	0.3570
QSFP DD (Mid)	Lane 9	0.3700	0.3730
	Lane 10	0.3705	0.3735
	Lane 11	0.3705	0.3735
	Lane 12	0.3220	0.3250
	Lane 13	0.4190	0.4220
	Lane 14	0.4835	0.4865
	Lane 15	0.4995	0.5025
	Lane 16	0.4835	0.4865
QSFP DD (Top)	Lane 17	0.4350	0.4380
	Lane 18	0.4025	0.4055
	Lane 19	0.4835	0.4865
	Lane 20	0.4670	0.4700

\* All measurements were performed with 31ps accuracy using LDA's Time-Of-Flight Latency Measurement solution.





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